REMARKS

Rejection of Claim 1 Under 35 U.S.C. §103(a), *Hsue* (5,378,654) in view of *Chang et al.* (5,893,740).

Reconsideration of the rejection of claim 1 is respectfully requested.

The invention of claim 1 is directed to a method of forming a contact hole without forming an etch stop liner. The contact hole is self-aligned with respect to a transistor gate having a gate length less than 0.2 microns.

As is well known, the Examiner bears the burden of establishing a prima facie case of obviousness based upon the prior art. This burden is satisfied only by showing some objective teaching in the prior art or knowledge generally available to one of ordinary skill in the art to combine the relevant teachings.[1]

A prima facie case is not believed to exist because the proposed substitution of the combination renders the prior art unsatisfactory for its intended purpose. In addition, Applicants have submitted additional evidence arguing against the proposed combination.

There is no motivation to combine the references because the transistor of *Chang et al.* is not compatible with the process of *Hsue*. The reference *Hsue* is directed to a self-aligned contact (SAC) process. *Hsue* teaches a stacked gate electrode with a gate dielectric layer.[2] In the SAC process of *Hsue*, a gate dielectric layer is formed on a conductive gate to prevent the conductive gate from being exposed during a self-aligned contact (SAC) etch.[3] A gate dielectric layer and sidewalls insulate the conductive gate from a subsequently formed conductive contact.[4]

Chang et al. is not compatible with the *Hsue* process. *Chang et al.* teaches a short channel field effect transistor that does not include an insulating or dielectric layer

---

[1] In re Fine, 5 USPQ 2d 1596, 1598 (Fed. Cir. 1998).

[2] See *Hsue* FIG. 1A, item **14** and FIG. 2A item **44**.

[3] See *Hsue*, FIGS. 1E and 2C, which shows how layer (**14** or **44**) prevents polysilicon/polycide layer (**12** or **42**) from being exposed when a contact hole is etched.

[4] See *Hsue*, FIG. 1F, which shows a sidewall **18** and gate dielectric **14** that insulate gate **12** from contact **28**. See also, FIG. 2D, which shows a sidewall **48** and gate dielectric **44** that insulate gate **42** from contact **58**.

formed on the top of the gate.[5] Incorporating the transistor of *Chang et al.* into the *Hsue* process would entirely defeat the SAC process, as no structure would exist to prevent the gate from being exposed when the contact hole is etched. There is no structure that would insulate the conductive gate from a subsequently formed conductive contact.

Incorporating the gate of *Chang et al.* into the process of *Hsue* would necessarily require some additional steps not shown or suggested in either reference. In addition, Applicants respectfully note that the transistor of *Chang et al.* has many particular features that would have to be addressed were it to be incorporated into a SAC type process. Just of few of these features include particular ion implantation doses to form short channel source and drain regions, as well as a tilt ion implantation step that necessarily requires a silicide layer on the top of the gate, as well as a particular sidewall on the gate.[6]

Accordingly, because the proposed modification of incorporating the transistor of *Chang et al.* into the process of *Hsue* would render the process unsatisfactory as a self-aligned contact etching process, the prior art does not suggest the claimed invention, and this ground for rejection is not sustainable.

Applicants have previously emphasized the differences in teachings between *Hsue* and the claimed invention. In particular, it has been stressed that Applicants' invention is directed to contact formation for smaller geometry devices (i.e., gate lengths of less than 0.2 microns), while *Hsue* appears directed to large geometry devices, and so is not suggestive of Applicants' smaller geometry claim limitations.[7] In previous Responses to Office Action, Applicants have noted that the background art for conventional smaller

---

[5] See *Chang et al.*, FIG. 1(b) and 3(b), which show a silicide layer formed on the top of the gate electrode. No dielectric layer is formed on the gate.

[6] See *Chang et al.*, Col. 3, Lines 49-54 and FIGS. 1(c) and 3(c).

[7] See *Hsue*, FIGS. 2A and 2B, and accompanying descriptions in Col. 3 and 4. In particular, Col. 3, Lines 65-67 indicate a polysilicon/polycide layer **42** has a thickness of about 3,000 Å. A silicon dioxide layer **46** has a thickness of about 2,500 Å. FIGS. 2A and 2B thus appear to be drawn close to scale. A measurement of the gate length in FIGS. 2A and 2B yields a length of about 8,000 Å, which equals 0.8 μm. Applicant's claim 1 limitations recite a gate of length less than 0.2 μm.

geometry contact approaches include an etch stop liner.[8] When Applicants' Specification was apparently not sufficient to establish such teachings in the art, a reference *Jeng et al.* (U.S. Patent 6,033,962) was submitted that repeats teachings of the Background Art in the Specification. No rebuttal was offered in response to this submission.

To more clearly indicate why one skilled in the art would not turn to the large geometry method of *Hsue* for solving the small geometry issues of the claimed invention, Applicants hereby submit additional references that clearly indicate that conventional small geometry approaches include protective liners, as noted in the Background Art. Relevant portions of these references are included in Appendix A.[9] These references, due to their filing dates are not prior art, and are simply cumulative of the Background Art of the Specification.

For all of these reasons, it is believed that a prima facie case of obviousness has not been established, and this ground for rejection should be withdrawn.

Rejection of Claim 12 Under 35 U.S.C. §103(a), *Hsue* (5,378,654) in view of *Chang et al.* (5,893,740).

To the extent that this ground for rejection relies upon the combination of *Hsue* in view of *Chang et al.*, the arguments set forth regarding claim 1 are incorporated by reference herein. Namely, the combination is improper, as it would render the prior art unsuitable for its intended purpose.

In addition, a prima facie case of obviousness has not been established, as the combination of references does not show all limitations of the claim.

---

[8] See the Response to Office Action, Filed December 22, 2000, Page 4, Footnote 4, and the Response to Office Action, Filed June 14, 2001, Page 2, Footnote 1.

[9] See *Jang et al.* (U.S. Patent 6,297,162), Col. 1, Lines 38-53, which indicate that for closely spaced MOS gates, a SAC contact must be formed that includes an etching stop (i.e., a liner) to prevent plasma etch from damaging the substrate surface. See also, *Hirohama* (U.S. Patent No. 6,245,621), Col. 1, Lines 21-25, which indicates that for gate electrodes reduced to 0.25 micron or less, it is difficult to form contacts. See also, Col. 1, Lines 57-59, which indicates that one of the problems is that dry etching causes damage on the semiconductor substrate.

Claim 12 is directed to a method of etching a contact hole through a first insulating layer of doped silicon dioxide. The etching is with an etch selectivity between the first insulating layer and sidewall that is greater than ten to one, and between the first insulating layer and substrate that is greater than one hundred to one.

The references do not show or suggest a first insulating layer of doped silicon dioxide. *Chang et al.* provides no teachings whatsoever regarding insulating layers, and so cannot be suggestive of the doped first insulating layer as recited in claim 12.

Hsue does not show a first insulating layer of doped silicon dioxide.[10] Further, because all examples of *Hsue* are for undoped silicon dioxide, it is not understood how the reference can be suggestive of the doped first insulating layer of claim 12.

It is noted that no argument has been provided to explain how this limitation is shown or suggested by the references.

The references do not show or suggest the two etch selectivity limitations of claim 12. *Chang et al.* provides no etch teachings whatsoever, and so cannot be suggestive of the etch selectivities of claim 12.

Hsue does not describe any particular etch selectivity in the formation of a contact hole.[11] The rejection of claim 12 appears to based on the argument that the etch selectivities of claim 12 are inherent in *Hsue*. The argument is set forth below.

> [U]sing the etching method, oxide insulating layer and insulating sidewall materials of Hsue, which are the same as those of the claimed invention would inherently result in obtaining the same

[10] See *Hsue*, FIG. 1C and description at Col. 1, Lines 54 to 66, which describe the formation of a spacer **18** from a layer of CVD silicon dioxide. See also FIG. 1D and description at Col. 2, Lines 3-8, which indicates layer **21** is also CVD silicon dioxide. These layers are not described as being doped.

[11] See *Hsue*, Col. 2, Lines 16-19, which describes a SAC etch of plasma etching with a conventional anisotropic oxide etchant. See also, Col. 4, Lines 36-40, which describes a reactive ion etch with an oxide etcher. No etch selectivities are described.

etch selectivities as claimed in the present invention for the purposes of obtaining the best etched product.[12]

It is clear that the argument relies on incorrect facts. The insulating and sidewall materials of *Hsue* are not the same as Applicants' claim 12. Applicants' claim 12 includes a first layer comprising doped silicon dioxide. *Hsue* shows no doping at all.

Because the cited references do not show or suggest all limitations of claim 12, a prima facie case of obviousness has not been established, and this ground for rejection should be withdrawn.

Rejection of Claim 18 Under 35 U.S.C. §103(a), *Hsue* (5,378,654) in view of *Chang et al.* (5,893,740), further in view of *Avanzino et al.* (5,776,834).

To the extent that this ground for rejection relies upon the combination of *Hsue* in view of *Chang et al.*, the arguments set forth regarding claim 1 are incorporated by reference herein.

In addition, the arguments set forth regarding claim 12 are incorporated by reference herein. Namely, the combination of *Hsue* in view of *Chang et al.* does not show or suggest a doped insulating layer, as recited in claim 18.

Claim 18 is directed to a method that includes forming a hard mask of substantially undoped silicate glass over an insulating layer comprising doped silicon dioxide. In addition, a contact hole is formed through the insulating layer between conducting structures separated by one another by less than 0.4 microns. The contact hole is formed without forming a protective liner over the conducting structures.

In addition to the various reasons noted above, the rejection of claim 18 is not sustainable, as the rejection relies on an improper standard. In rebutting Applicants' argument that motivation for the combination of references does not exist, the rejection states:

[12] See the Final Office Action, dated 8/16/01, Page 9, Lines 2-5.

In this case, it would have been obvious to one having ordinary skill in the art to modify Hsue in view of Chang by using conductive lines that are less than 0.5 microns or less as taught by Avanzino *for the purpose of obtaining the claimed invention* (emphasis added).

The above analysis is the definition of hindsight. Modifying a reference for purpose of obtaining Applicants' invention follows an approach expressly inhibited by numerous decisions. It is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious.[13]

For all of these reasons, reconsideration of the rejection of claim 18 is respectfully requested.

The present claims 1-14 and 16-19 are believed to be in allowable form. It is respectfully requested that the various grounds for rejection be reconsidered, and the application be forwarded for allowance and issue.

Respectfully Submitted,

Bradley T. Sako 10/16/01
Bradley T. Sako
Reg. No. 37,923

Bradley T. Sako
Attorney/Agent
3954 Loch Lomand Way
Livermore, CA 94550
Tel. 1-408-839-1082
Fax 1-925-961-0184

[13] In re Fritch, 23 USPQ 2d 1780, 1784 (Fed. Cir. 1992).

APPENDIX A